

1. Title of the Invention

RECORDING FORMAT FOR INFORMATION DATA,
INFORMATION RECORDING/REPRODUCING CODING CIRCUIT

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2. Background of the Invention

Field of the Invention

The present invention relates to a recording format for information data, an information recording/reproducing coding method, an information recording/reproducing encoding circuit, a magnetic recording/reproducing apparatus using these, an information recording/reproducing apparatus and an information communication device respectively for recording/reproducing an information data code at high speed and at high reliability in a high-density mass-storage information recording/reproducing apparatus by magnetic recording and optical recording medium.

Description of the Related Art

To realize information recording system at high speed and at high recording density, signal processing technique for faithfully reproducing information recorded on a recording medium plays an important role. Above all, in a mass-storage memory device represented by a high-density magnetic recording/reproducing apparatus, not only to secure the reliability of data recorded for a long term but to prevent various noise disturbance caused by high-density recording and the

quality deterioration of recorded/reproduced signal caused by the minuteness of a recorded element due to high-density recording and realize lower-cost and high-density information recording apparatus , higher-
5 precision data conversion technique from a recorded/reproduced signal to information data is desired.

For signal processing technique developed as technique for solving the above-mentioned technical
10 problems and currently applied to magnetic disk products widely, there is a PRML technique in which a partial-response equalization method and a maximum-likelihood decoding method are combined, for example, a method of embodiment is disclosed in detail in a
15 nonpatent reference document 1, "A PRML System for Digital Magnetic Recording" (IEEE Journal of Selected Areas on Communications, vol. 10, pp. 38 to 56, January 1992) and demodulation from a reproduced signal to data at lower signal-to-noise (SN) ratio is enabled by
20 disclosed technique, relieving the problem of intersymbol interference caused by high-density recording.

In the meantime, for a method to keep the data reliability in a general memory device, means for
25 correcting code errors caused in reproduced data by using error-correction coding technique is widely known and a coding method based upon classical algebraic code system, above all, error-correction coding technique

such as Reed-Solomon code is most widely applied to a mass-storage recording device. The Reed-Solomon code can correct the predetermined number of code errors caused in a reproduced code sequence in units of code symbol of predetermined bit length by adding a redundant code symbol for checking the code errors into a recorded code sequence beforehand.

Generally, in case the code symbol unit has n-bit length, a code sequence composed of maximum $2^{(n-1)}$ symbols can be formed and arbitrary t pieces of error symbols in the code sequence can be corrected by adding $2t$ pieces of redundant code symbols. As described above, as guaranty for error correction for a reproduced code sequence can be easily defined using a Reed-Solomon code that can set maximum correction capability in units of symbol maximum number of correctable error symbol and powerful error-correction processing in which an arbitrary code error event within the maximum number of corrected symbols can be corrected can be realized, the Reed-Solomon code is widely applied to a recording device and for general technique for guaranteeing the reliability of data, the Reed-Solomon code greatly contributes to high-density information recording.

However, to realize further higher-density recording, the increase of code error allowable capability by the enhancement of error-correction coding technique is required. To enhance the error-

correction capability, a method of increasing the number of redundant code symbols is easy, however, in the meantime, in information recording, as the increase of redundant code symbols requires the further increase 5 of effective recording density, the method itself is in a limited use.

For another method of enhancing the capability of error-correction coding without increasing redundant code symbols, there is an error-correction decoding 10 method using soft-output information and for new coding technique in which maximum-likelihood decoding by soft-output iterative decoding is executed corresponding to error-correction coding, recently the application of error-correction technique by Turbo coding has been 15 introduced mainly to a data communication field. The Turbo coding technique was proposed by C. Berrou and others in 1993 and is disclosed in a nonpatent reference document 2, "Near Shannon Limit Error-Correcting Coding and Decoding: Turbo-codes" (IEEE 20 Proceedings of International Conference on Communications, pp. 1064 to 1070, May 1993) for example.

The Turbo coding technique executes a concatenated coding that plural code sequences acquired by permuting (interleaving) the same information code 25 sequence at random are generated, simple error-correction coding to generate is applied to each of the plural code sequences and the plural redundant codes are added to the information code sequence. Besides,

in decoding, the technique executes an iterative
technique that soft-output decoding is individually
executed using each of the plural redundant codes for
error-correction coding, when one soft-output decoding
5 is executed, the result of maximum-likelihood code
sequences for the whole code sequence can be gradually
acquired by executing iterative decoding utilizing the
results of the other soft-output decoding as the prior
information of each code. As described above, the
10 Turbo coding technique is provided with means for
realizing optimum decoding for random coding and is
technique highlighted as a method of coding and
decoding for transmission for realizing a coding gain
close to Shannon limit bound on realistic circuit scale.
15 Similarly, a random code error caused in a reproduced
code sequence can be powerfully corrected by applying
the technique to a recording/reproduction system of an
information recording apparatus and it can be expected
that a gain limit of near optimum by the addition of
20 code redundancy is achieved on realistic hardware scale
and at realistic speed.

However, in an actual magnetic
recording/reproducing apparatus, as a defect which may
exist on a magnetic recording medium and a continuous
25 bursty signal defect caused by the accidental touch of
a magnetic head/medium system exist in addition to a
random code error caused by noise, means for
efficiently improving both factors of code errors by

both is required. In such signal environment, in the above-mentioned Turbo coding technique, the above-mentioned principle effectively acts on the former random code error and extremely high code correcting 5 capability can be fulfilled, however, in the meantime, for the latter burst defect, as the soft-output information of an individual code cannot be suitably generated, the proper correcting capability cannot be fulfilled. Or a code error cannot be also extremely 10 rarely corrected for the superimposition of specific random noise and in these cases, a code error is finally diffused (propagated) and increased in the whole code sequence due to the random permutation (interleave) of an information code sequence.

15 Besides, in a patent document 1 (Japanese published unexamined patent application No. 2001-285080), a decoder that detects loss in decoding using a convolutional interleaver is disclosed, however, means for solving the above-mentioned problems is not 20 provided.

In such a situation of the prior art, even if error-correction means based upon the Reed-Solomon code is added, the recovery of data cannot be guaranteed and it is extremely difficult to apply the 25 Turbo coding principle in configuration heretofore disclosed to a mass-storage recording/reproduction device for which reliable data integrity is required. Besides, in coding/decoding means by hard-decision

algebraic means such as the Reed-Solomon code, the correctable number of correctable code errors is disclosed beforehand and code design is enabled, however, in Turbo coding, as error detection/correction 5 are executed based upon soft-output information, the correctable number of code errors cannot be disclosed. This makes the reliable design of a data recording/reproduction device for enhancing high recording density and high-speed data transfer rate in 10 the prior art extremely difficult and makes the application of Turbo coding to the device more difficult.

[Nonpatent document 1]

"A PRML System for Digital Magnetic Recording" 15 (IEEE Journal of Selected Areas on Communications, vol. 10, pp. 38 to 56, January 1992)

[Nonpatent document 2]

"Near Shannon Limit Error-Correcting Coding and Decoding: Turbo-codes" (IEEE Proceedings of 20 International Conference on Communications, pp. 1064 to 1070, May 1993)

[Patent document 1]

Japanese published unexamined patent application
No. 2001-285080

25 3. Brief Summary of the Invention

The object of the invention is to apply the above-mentioned principle of Turbo coding to a high-density high-speed information recording/reproduction

system represented by a magnetic recording/reproduction apparatus, to enhance error-correction ability in recording/reproduction and to realize the further enhancement of the high recording density and high-speed data transfer rate of information recording.

5 The invention is made to solve the realistic problems in applying the principle of Turbo coding to the high-density high-speed information recording/reproduction apparatus. That is, one object 10 of the invention is to enhance correction capability for the above-mentioned two code error modes existing in real recording/reproduction apparatus by solving the problem of code error propagation due to the failure of error correction in Turbo coding and in addition, 15 providing error correction coding system configuration in which correction capability for a burst error mixed in a random error can be guaranteed. The further problem the invention is to solve is the deterioration of the latency of data decoding by iterative processing 20 in decoding. A decoding principle in Turbo coding in which decoding is repeated for a code sequence including operation for permuting the whole information code sequence causes decoding time delay equivalent to a few times of the information code sequence. Such a 25 problem is a very significant problem to realize high-speed data transmission in a recording/reproduction apparatus.

The object of the invention is to solve the

above-mentioned decoding latency problems and to provide a recording format for information data, information recording coding method and circuit, a magnetic recording/reproduction apparatus using them, 5 an information recording/reproduction apparatus and an information communication device respectively provided with more powerful and high-speed error-correction coding means applying the principle of Turbo coding.

To achieve the above-mentioned objects, the 10 invention is based upon a magnetic recording/reproduction apparatus and is characterized in that a recording format for recording information data on a recording medium includes a preamble including additional information for the control of 15 recording positional information, signal amplitude gain control and data timing recovery, an information code composed of code blocks including a second redundant code bit (a second parity code bit) and a common-length redundant code composed of code blocks including a 20 first redundant code bit (a first parity code bit) and the length of each code block including the redundant code bit of the second redundant code is equal to the length of a code symbol (unit) correctable by the first redundant code bit or shorter.

25 Besides, the invention is based upon an information recording/reproducing coding method for recording an information code sequence to which error-correction coding for detecting and correcting a code

error caused in the information code sequence
reproduced from an information recording medium is
applied on the information recording medium, and is
characterized in that error correction in units of
5 predetermined code (code symbol) is applied to a unit
(an information data sector) of an information code
sequence once recorded on the information recording
medium, first error-correction coding for correcting
error code symbols caused in the corresponding
10 reproduced information data sector up to a
predetermined number of correctable error code symbols
is applied, a redundant code sequence by the first
error-correction coding is added into the corresponding
information data sector, the information data sector to
15 which the first error-correction coding is applied is
divided into consecutive plural code sequence blocks
with a predetermined code symbol length, second error-
correction coding is applied to each code sequence
block, a redundant code by the second error-correction
20 coding this is inserted into the corresponding code
sequence block, the code sequence block to which the
second error-correction coding is applied has code
sequence block length in units of code symbol in the
first error-correction coding and an information code
25 sequence to which error-correction coding is applied
and which has the code sequence block length equal to
or shorter than the number of code symbols correctable
by the first error-correction coding is recorded on the

information recording medium.

Further, the invention is based upon an information recording/reproducing encoding circuit provided with an error-correction encoding circuit for 5 detecting and correcting code errors caused in the information code sequence recorded onto the information recording medium when the information code sequence is reproduced from an information recording medium and is characterized in that error correction in a 10 predetermined code unit (code symbol) is executed in a unit (an information data sector) of information code sequences once recorded on the information recording medium, an encoding circuit for executing first error-correction coding for correcting error code symbols 15 caused in the reproduced information data sector up to a predetermined number of correctable error code symbols is provided, a redundant code sequence by the first error-correction coding is added to the information data sector output by this, a circuit for 20 dividing the code contents of an information data sector code sequence output from the encoding circuit for executing the first error-correction coding into consecutive plural code sequence blocks with a predetermined code symbol length and holding each code 25 sequence block is provided, an encoding circuit for executing second error-correction coding, referring to the code contents of each code sequence block and an error-correction encoding circuit having code sequence

block length to which the second error-correction
coding is applied in units of code symbol in the first
error-correction coding and which is equal to or
shorter than the number of code symbols correctable by
5 the first error-correction coding for outputting a
series of code sequence blocks as a code sequence
recorded on the information recording medium after a
redundant code output from each second encoding circuit
is inserted into the corresponding code sequence block
10 are provided, wherein the code sequence block has a
code length to which the second error-correction coding
is applied in units of code symbol in the first error-
correction coding and which is equal to or shorter than
the number of code symbols correctable by the first
15 error correction coding, and a code sequence for
recording on the information recording medium to which
an information code sequence is converted by the error-
correction encoding circuit is output.

Furthermore, the invention is characterized in
20 that the above-mentioned circuit is mounted in a
magnetic recording/reproduction apparatus, an
information recording/reproduction apparatus and an
information communication device.

4. Brief Description of the Drawings

25 Fig. 1 shows an example of the whole
configuration of an information recording/reproduction
system according to the invention;

Fig. 2 shows an example of the configuration of a

recording encoder (an encoding circuit in recording) according to the invention;

5 Fig. 3 shows an example of a recording format for information data of an information recording sector in a magnetic recording/reproduction apparatus according to the invention;

Fig. 4 shows an example of an error-correction decoder (an error-correction encoding circuit in decoding) according to the invention;

10 Fig. 5 shows an example of an error-correction encoding circuit (a random interleaver/deinterleaver) in recording according to the invention;

Fig. 6 is a trellis diagram used for a parity decoder (decoding circuit) according to the invention;

15 Fig. 7 shows an example of the configuration of a convolutional code of a code redundancy arrangement (redundancy circuit) according to the invention;

Fig. 8 shows an example of the configuration of a recording encoder (encoding circuit) according to the invention;

20 Fig. 9 shows an example of another configuration of the recording encoder (encoding circuit) according to the invention;

Fig. 10 shows an example of another configuration 25 of the error-correction decoder (the error-correction encoding circuit in decoding) according to the invention;

Fig. 11 shows an example of further another

configuration of the recording encoder (encoding circuit) according to the invention;

Fig. 12 shows an example of further another configuration of the error-correction decoder (the error-correction encoding circuit in decoding) according to the invention;

Fig. 13 shows an example of the configuration of the magnetic recording/reproduction apparatus according to the invention; and

Fig. 14 shows another example of the recording format for information data of the information recording sector in the magnetic recording/reproduction apparatus according to the invention.

5. Detailed Description of the Preferred Embodiments

First, the outline of an information recording/reproduction encoding method according to the invention will be described. In the information recording/reproduction encoding method according to the invention, coding for effectively correcting both of a random code error and a burst error is executed by concatenating by a Turbo coding configuration and a hard-decision Reed-Solomon code configuration. Further, in the invention, first error-correction coding that burst errors with a predetermined maximum length in the whole information data sector (in units of recorded/reproduced code information symbol) are corrected by a hard-decision Reed-Solomon code based upon predetermined redundancy and concatenated coding

(second error-correction coding) that the whole information data sector is divided into plural code blocks and Turbo coding is applied to each code block are executed. As described above, when Turbo coding is 5 applied to a divided block, a code error can be limited to a range of a code block even if the bursty propagation of the code error is caused by the failure of the code error correction based upon soft-output information in Turbo decoding. Therefore, an event of 10 the propagation of the code error by Turbo coding can be securely recovered by limiting the size of the code block within the maximum correctable error number of a burst (first) error-correction code added in the corresponding sector. Besides, the decoding delay of 15 soft-output iterative decoding applied to each code block can be reduced by applying Turbo coding to a shorter code block divided in plurality.

In error correction by the above-mentioned coding, in case the correction by the first error-correction 20 coding for a burst error fails, securer data reproduction is enabled by feedbacking already acquired soft-output coding information to acquire further powerful error-correction effect and newly generating soft-output information based upon a reproduced signal. 25 As a result of soft-output decoding by the second error-correction coding, the likely code information of most of codes dispersed in the whole sector is acquired, and the generation of higher-reliable soft-output

information and the reduction of code errors are enabled by utilizing the likely code information together with newly input reproduced signal information and using it as prior code information because the
5 effect of burst error distortion is small owing to dispersion in the whole wider sector. Such iterative decoding in units of sector excessively increases decoding delay time, however, as the rereading of data (retry operation) is performed as in the invention only
10 in case error correction by the first error-correction coding is impossible, the effective data reading time (data latency) of a storage device can be remarkably reduced by iterative processing.

An encoding circuit using the above-mentioned
15 error-correction coding method and decoding method is provided with means that can set the individual frequency (iteration) number and the maximum frequency (iteration) number of iterative decoding and has the following characteristics.

20 (1) When signal amplitude loss (dropout) of predetermined code length is added to a reproduced signal sequence supplied from a recording medium and a continuous error is caused in an information code sequence or when a set iterative frequency is increased,
25 time since the reproduced signal sequence is input until the result of the decoding of an information code sequence for the reproduced signal sequence is output increases.

(2) In case signal amplitude loss (dropout) of predetermined code length is added to the reproduced signal sequence supplied from the recording medium and the continuous error is caused, the predetermined code length exceeds a certain value equal to or shorter than code sequence block length when the detection and the correction of a code error by the first error-correction coding are impossible, a code error caused as the result of the decoding of the information code sequence is longer than the length of the signal amplitude loss (dropout) and is limited to length equal to or shorter than the code sequence block length.

(3) The encoding circuit is characterized in that in the detection and the correction of a code error by the first error-correction coding, when a flag showing that an error-correction code is impossible is transmitted or when a retry mode is used, time since the reproduced signal sequence is input until the result of the decoding of the information code sequence for the reproduced signal sequence is output increases. The increase of the time varies in units of the length of time in which the contents of codes in the corresponding information data sector are output or shorter. It is validated based upon such characteristics that code error-correction means by the above-mentioned encoding means is provided. Referring to the drawings, embodiments of the invention will be described in detail below.

First Embodiment

Fig. 1 shows an example of the whole configuration of an information recording/reproducing system for embodying the invention. The invention is embodied in a recording/reproducing signal processing circuit 1 for recording/reproducing an information code on a head/recording medium system 200 in a high-density mass-storage magnetic recording/reproducing apparatus (a magnetic disk unit) at high reliability. The invention can be applied not only to the magnetic disk unit but to a high-density mass-storage recording/reproducing apparatus using magnetic recording/optical recording/photomagnetic recording. The recording/reproducing signal processing circuit 1 shown in Fig. 1 is generally realized in the configuration of a large-scale semiconductor integrated (LSI) circuit device, and its basic function is composed of two processes of a recording system 100 that converts recording code information 101 to write current 105 and supplies it to the head/recording medium system 200 and a reproduction system 300 for converting a reproduced signal 305 from the head/recording medium system 200 to reproduced code information 301. The invention is characterized in that a recording/reproducing method including a practical information recording/reproducing coding method based upon Turbo coding principle is provided to a method of converting the recording code information

101 in the recording system 100 and a method of
converting to the reproduced code information 301 in
the reproduction system 300 to reduce as many code
errors as possible in reproducing information in the
5 reproduction system 300 and to demodulate the
reproduced code information 301 at higher reliability.
The invention is also characterized in that the
invention realizes circuit means having concrete
configuration including an information
10 recording/reproducing encoding circuit for realizing
the recording/reproducing method for the
recording/reproducing signal processing circuit 1 and
also realizes a magnetic disk recording/reproducing
apparatus using this circuit, further an information
recording/reproducing apparatus and an information
15 communication device.

In the recording system 100, an information code
sequence 101 transmitted from a computer or a host
controller of periphery equipment is input and after it
20 is converted to a recording code sequence 103 in an
encoder (an encoding circuit) 102, the recording code
sequence is converted to a desired write current
sequence 105 in a write current conversion circuit 104.
In the write current conversion circuit 104, the
25 control in which a recording process in the
head/recording medium system 200 succeeding the write
current conversion circuit 104 is supposed of a write
current level and the compensation of the phase at a

point at which a suitable current level varies are performed and the write current sequence 105 output from the write current conversion circuit is supplied to a recording head in the head/recording medium system 5 200 via a write amplifier 106, and code information corresponding to the code information sequence 101 is physically recorded in a desired position on a magnetic disk recording medium (on an optical disk recording medium in the case of another information recording/reproducing apparatus, for example, in the 10 case of an optical disk recording/reproducing apparatus) via the recording head. The recorded code information is read from a desired recorded location at desired time by a reproducing head according to an 15 instruction from the host controller and is output as a reproduced signal sequence 305 which is an electric signal (the variation of voltage) via a read amplifier 306.

In the reproduction system 300, the reproduced 20 signal sequence 305 is input via the read amplifier (amplifying circuit) 306 and predetermined reproduced signal processing such as adjusting the amplitude of read voltage, filtering for removing noise, conversion from an analog signal to a digital signal and shaping 25 (equalizing) the waveform of a reproduced signal is applied to the reproduced signal sequence in a reproduced signal processing circuit 304. Particularly in the current high-density recording magnetic disk

unit, a principle of reproduced signal processing called partial response maximum likelihood (PRML) is generally used and this embodiment is also based upon the data reproducing method.

5 The details of this method are disclosed in the nonpatent reference document 1 for example. Generally, in PRML, an input analog reproduced signal is controlled so that it is at a desired signal level and after the signal is converted to a digitized and
10 quantized digital signal at the time interval of an information code bit, partial response equalization processing (intersymbol interference control) by a digital filter and the detection of reproduced code information by a maximum-likelihood decoder (a decoding circuit) are performed. In this embodiment, a signal process for generating a decoded signal sequence 303 (generally, a digital signal sequence) which is an output for partial response equalization from the input of the analog reproduced signal immediately before the
15 detection of reproduced code information is executed in the reproduced signal processing circuit 304.

20 Further, in the reproduction system 300, the decoded signal sequence 303 output from the reproduced signal processing circuit 304 is converted to a reproduced code sequence 301 corresponding to an original information code sequence 101 via a decoder (a decoding circuit) 302. At this time, in the decoder (the decoding circuit) 302, data soft-output decoding
25

by the maximum-likelihood decoder and error detecting/correcting decoding utilizing error detecting/correcting coding proper to the invention executed in the encoder 102 are executed.

5 The error detecting/correcting coding and the error detecting/correcting decoding will be described in detail in embodiments succeeding an embodiment shown in Fig. 2. As described above, the flow of processing in the recording system 100 is equivalent to the
10 reverse flow of processing in the reproduction system 300, and the encoder 102 and the decoder 302 and the recording signal processing circuit 104 and the reproduced signal processing circuit 304 are functionally relative. A series of flow from the
15 information code sequence 101 to the reproduced code sequence 301 can completely correspond to a series of flow of processing in a data communication system and the basic flow in the invention can be also applied to the communication system, that is, an information
20 communication device by replacing the head/recording medium system 200 with an information transmission system.

25 In the invention, a method of realizing conversion and reconstitution from the information code sequence 101 to the reproduced code sequence 301 at higher precision and reliability and compensating the data deterioration due to various disturbance in the head/recording medium system 200 of the signal quality

of the reproduced signal sequence 305 from the recording medium and the prevention of the faithful recording/reproduction (transmission) of information or a method of recording information on the medium at 5 higher density (transmitting data at high speed) and a circuit embodying this are realized. To embody this, in the invention, for a circuit for embodying a method of more mightily detecting/correcting a code error caused in the reproduced code sequence 301, a code 10 error detecting/correcting circuit based upon Turbo coding/decoding principle is provided in the encoder 102 and the decoder 302.

Turbo coding/decoding is known as a coding method showing performance near to Shannon limit bound for the 15 capacity of a channel which is the theoretical limit of coding performance, and the principle and the configuration of coding/decoding by a parallel concatenated convolutional code are disclosed in the nonpatent document 2 ("Near Shannon limit error 20 correcting coding and decoding": Turbo codes (I), in Proc. ICC'93, May 1993, pp. 1064 to 1070) by C. Berrou and others. The coding by the concatenated convolutional code is executed by a system that concatenates two convolutional encoders via an large 25 interleaver equal to the length of a code in units of information transmission. Decoding by the concatenated convolutional code is executed using a system composed of two encoding circuits for inputting/outputting soft-

output code information, the system executes iterative decoding that the soft-output information of each code is repeatedly exchanged between the two decoding circuits and acquires the final result of decoding.

5 Such soft-output interactive decoding can effectively realize maximum-likelihood decoding for concatenated coding and can realize the maximum-likelihood decoding of a code sequence.

The invention provides means for realizing the principle of Turbo coding/decoding by the encoder 102 and the decoder 302 and greatly enhancing the reliability of recording/reproducing the information code sequence and simultaneously provides the concrete method and the concrete circuits for recovering the 15 failure of code error correction in Turbo coding/decoding caused by disturbance such as various noise which may occur in an actual information recording/reproducing apparatus and keeping the information recording/reproducing apparatus at a higher 20 reliability. Besides, the invention simultaneously provides a method and a circuit for reducing the delay of decoding by iterative decoding to a practical extent and a recording format for information data for them.

Generally, in Turbo coding/decoding, iterative decoding is executed using soft-output code information and at this time, the similar permutation (the shuffling) of code information to interleave used in coding is performed between the decoding. In well-

known Turbo coding, as the permutation is executed in units of the whole codes (data sector), the iterative decoding does not converge in case the superimposition of unusual noise occurs at an extremely rare 5 probability and a phenomenon that a code error diffuses (propagation) may occur. This is a phenomenon which may occur at a significant probability depending upon the configuration of a code even in a relatively satisfactory noise condition and can be observed as an 10 error saturation characteristic called an error floor in an error rate characteristic. In such a coding system, even if the signal-to-noise (SN) ratio quality of a reproduced signal can be improved, information 15 cannot be reproduced at reliability equal to or less than the error saturation characteristic.

As the soft-output decoding uses soft-output code information supposing the superimposition of random noise, it is extremely weak in the continuous signal deterioration such as the continuous amplitude loss 20 (dropout) of a continuous reproduced signal caused by a burst defect on the recording medium and the abnormal variation and offset of a level and in this case, a code error is also magnified. For means for reconditioning such a situation, a method of 25 concatenating hard-decision algebraic block codes such as a Reed-Solomon code is conceivable together with Turbo coding, however, as in normal concatenated coding, a range of the diffusion (propagation) of a code in

permutation by Turbo decoding is large, the propagated errors cannot be securely covered and the concatenated coding does not work for such situation. To solve this problem, in the invention, coding and decoding in the 5 following embodiments are executed in the encoder 102 and the decoder 302.

Second Embodiment

Fig. 2 shows an example of the configuration of the encoder (the encoding circuit in recording) 102 according to the invention. The encoder 102 is 10 provided with an error-correction encoder (an error-correction encoding circuit) 10 for applying algebraic error-correction coding (first error-correction coding) by a Reed-Solomon code to an input information code sequence 101 and the error-correction encoder outputs 15 an error-correction code sequence 11. In actual recording coding, recording modulation coding that a specific code constraint condition such as code run-length constraint is added to write data code sequence 20 is required to be executed to guarantee the extraction of amplitude gain control/data timing recovery information from a reproduced signal, to inhibit a DC component in a recorded/reproduced signal or to remove 25 a recording code pattern in which a reproduction error may occur beforehand, and a recording code modulator (a modulation circuit) 12 is provided to apply the coding conversion to the error-correction code sequence 11.

Further, a recording modulated code sequence 13

output from the recording code modulator 12 is input to a concatenated encoder (an encoding circuit that executes second error-correction coding) 14. The concatenated encoder 14 applies the second error-
5 correction coding based upon a principle of Turbo coding to the recording modulated code sequence 13. The concatenated encoder 14 generates a predetermined redundant code based upon the input code sequence and also generates the similar redundant code based upon a
10 new code sequence formed by rearranging the input code sequence. Therefore, the recording modulated code sequence 13 input to the concatenated encoder 14 is stored in a code buffer circuit 15c for holding the contents of a code sequence of predetermined code block
15 length and the contents are held in recording buffer circuits 15a and 15b for changing the code bit position of the code sequence in fixed order and holding it. A circuit composed of the recording buffer circuits 15a and 15b for permuting a code is called a random
20 interleaver 15 and generally, the contents of the code are rearranged according to a one to one code mapping rule with the length of a code sequence unchanged.

Turbo coding is characterized in that error-correction coding is applied to a sequence acquired by
25 rearranging the same code sequence in different order via the interleaver. For a code mapping rule at this time, rearrangement in random order or rearrangement under a predetermined constraint condition is set,

however, in a decoder 300 described later corresponding to one encoder, an unchanged code mapping rule is set. A specific conversion rule may be set depending on a code error event caused by the head/recording medium system 200 and a data transmission system, however, in the embodiment of the invention, this is not caused. In the concatenated encoder 14, referring to the contents of the code held in the recording buffer circuits 15a and 15b, a redundant code bit is generated by redundant encoders 16a and 16b.

In this embodiment, for the redundant encoders 16a and 16b (an encoding circuit that executes the second error-correction coding, in this case, a redundant bit is a redundant code output from these encoding circuits), a parity check coding method having the simplest configuration is disclosed, however, basically, for the configuration of the redundant encoder, the configuration of a recursive convolutional encoder is adopted. In the invention, each of the redundant encoders 16a and 16b is provided with each code delay element 17a, 17b and each exclusive-OR 18a, 18b with the next code is acquired by sequentially holding a 1-bit input code and feedbacking the contents. A parity check code bit is always held in the code delay elements 17a and 17b by sequentially applying this to an input code bit from the recording buffer circuits 15a and 15b (every time the reference of the contents of code information held in each recording

5 buffer circuit 15a, 15b is started, the contents of the code delay elements 17a and 17b are initialized, and until code information in each buffer is sequentially referred and a code bit at each trailing end is output to the redundant encoders 16a and 16b, the recursive coding is repeated).

10 A code switch (switching circuit) 20 inserts one bit every fixed cycle of redundant code bit sequences 19a and 19b into the following information code 19 at predetermined timing, referring to original code 15 stored in the recording buffer circuit 15 and sequentially outputting it and outputs as one recorded code sequence 103 (as described above, every time the output of the redundant code bit sequences 19a and 19b from each redundant encoder 16a, 16b is referred in the information code 19, the code delay element of the redundant encoder may be also reset). The coding is one type of punctured coding and the timing of the insertion of a redundant code bit at this time can be flexibly set according to set code redundancy. In such coding, systematic coding in which an original information code and the position of an inserted parity check code bit are definitely distinguished can be executed. The increase of redundancy is effective to enhance later error-correction ability, however, in the meantime, as the addition of code redundancy causes the effective loss of recording density, suitable amount of redundancy is

required to be set in an actual information recording apparatus.

Besides, the invention is characterized in that the length of a code permuted by random interleave is limited by suitably setting the length of the recording buffer circuits 15a and 15b, for example, information data sector size is reduced to the length of a code divided in plurality. Besides, in this embodiment, the case that the two redundant encoders 16a and 16b are used is disclosed, however, in case a single encoder or three or more encoders are provided in parallel, the invention can be also applied. In case a single redundant encoder is used, it is general that referring to the output of the redundant encoder 16b in this embodiment, coding is performed. In the case of three or more redundant encoders, referring to the contents to which different interleave code permutation is applied of the recording buffer 15b, the similar coding is executed in parallel.

20 Third Embodiment

Fig. 3 shows a format for coding a recording code sequence output from the encoder 102, that is, an example of a recording format for information data according to the invention. The unit (an information data sector) of an information code once stored on a recording medium 200 in the invention has configuration shown in Fig. 3. The whole information data sector includes a preamble 24 including additional information

for the control of recording positional information and
amplitude gain control/data timing recovery, an
information code 22 and a redundant code 23 including
the Reed-Solomon code (the first error-correction code)
5 added by the error-correction encoder 10 shown in Fig.
2 in the second embodiment at the end. The Reed-
Solomon code can encode the corresponding code sequence
in units of predetermined code symbol and can correct
the code symbols including error codes, up to a
10 predetermined number of correctable error code symbols,
which is located in an arbitrary position of the
information code 22 and the redundant code 23 on the
corresponding sector in error correction using the
redundant code 23.

15 The detection and the correction of arbitrary
errors to t pieces of symbols can be guaranteed by
adding the redundant code 23 having the symbol length
of $2t$ according to Reed-Solomon code error correction
in a general well-known decoding method when the
20 contents of a code on the information data sector are
reproduced, and in a case of erasure correction, can
identify a value of $2t$ pieces of symbols (one symbol is
normally composed of continuous plural bits in the
corresponding code sequence, for example, 8 to 10 code
25 bits).

Further, as shown in Fig. 3, the information code
22 and the redundant code 23 in the recording
information data sector are divided in units of plural

code blocks 22a and each code block 22a has code length corresponding to the memory size of the recording buffer circuits 15a and 15b shown in Fig. 2. In each code block, a redundant code bit 22b (a parity coding bit) by the second error-correction coding generated in the redundant encoders 16a and 16b is inserted. That is, in the invention, a code has configuration that first error-correction coding by the Reed-Solomon code and second error-correction coding by Turbo coding are concatenated with different code lengths. In this embodiment, the redundant code bit 22b is composed of plural parity coding bits forming an output parity from each redundant encoder 16a, 16b and code length in interleave code permutation processing between the recording buffer circuits 15a and 15b executed in each parity coding corresponds to each code block 22a.

In other words, the invention is characterized in that the recording information data sector (the information code 22 and the redundant code 23 based upon the Reed-Solomon code) is divided into plural code blocks 22a and the second error-correction coding (parity coding) is performed in units of divided individual code block 22a, and in case Turbo decoding is repeated between plural parity codes in each code block 22a, the diffusion and propagation of a code error in the failure of decoding is limited to the length of code block 22a at most. Therefore, if coding (redundant 2t pieces of symbols or more, in correction

for loss, t pieces of symbols or more) is performed so that the maximum number t of correctable symbols in a Reed-Solomon code added as the redundant code 23 is the block length or longer, a decoding error in the failure 5 of Turbo decoding can be finally corrected.

In the meantime, Turbo coding by parity coding in units of code block 22a into which the information data sector is divided as in the invention for normal Turbo coding having the whole information data sector as a 10 code configuration unit deteriorates the error rate of random error correction by iterative decoding at ratio inversely proportional to the length of a code configuration unit (the code block 22a), however, the correction ability for a burst propagated error can be 15 also compensated by limiting the length of a code configuration block to error length in which recovery by a Reed-Solomon code can be compensated in the failure of Turbo decoding as in the invention, supplementing the deterioration, and optimum 20 reliability can be realized in the whole data decoding system.

The unit (the information data sector) of an information code sequence once recorded on the information recording medium in the embodiment of the 25 invention has the following characteristics. (1) Error correction in a predetermined code unit (a code symbol) is performed, first error-correction coding for correcting code symbols including code errors up to the

predetermined number or less of code error symbols in the corresponding reproduced sector is executed and a redundant code sequence by this is added to the corresponding information data sector. (2) The 5 information data sector to which the first error-correction coding is applied is divided into continuous plural code sequence blocks having a predetermined length, second error-correction coding is applied to each code sequence block and after a redundant code by 10 this is inserted into the corresponding code sequence block, they are recorded on the corresponding information recording medium. (3) The code sequence block to which the second error-correction coding is applied has a code sequence block length in units of 15 code symbol in the first error-correction coding and has a code sequence block length equal to or less than the number of error code symbols which can be corrected by the first error-correction coding. The information code sequence to which the error-correction coding 20 having the above-mentioned features is applied is recorded on the information recording medium 200 or a circuit for applying the error-correction coding having the above-mentioned features is provided in the encoder 102.

25 At this time, in the second error-correction coding, a recorded code sequence by Turbo coding having features that code permutation processing having code length equal to the code sequence block as a processing

unit is applied to a code sequence corresponding to the above-mentioned code sequence block, plural code sequence blocks are generated, predetermined error-correction coding is applied to the generated plural 5 code sequence blocks and a redundant bit generated by each error-correction coding is inserted in a predetermined position in the corresponding code sequence block is configured. Therefore, the encoder is characterized in that a code permutation circuit 10 having a code length equal to the code sequence block as a processing unit and a memory circuit for holding the result of code permutation equal to the code sequence block are provided, an encoding circuit for applying the predetermined second error-correction 15 coding, referring to the contents of the plural memory circuits is provided and circuit means for inserting a redundant bit output by each encoding circuit in a predetermined position in the corresponding code sequence block held in the memory circuit beforehand is 20 provided.

In the third embodiment shown in Fig. 3, a redundant code bit (a parity coding bit) 22b added into each code block 22a is arranged at a fixed bit interval in the block. The parity coding arrangement in which 25 the parity redundant code bits 22b is separately distributed or scattered in each code block 22a may be helpful to prevent most of redundant code bits from simultaneously being deteriorated by a burst signal

defect localized at certain bit positions in the code block 22a. Meanwhile, as shown in Fig. 14, the redundant code bit may be collectively arranged in a predetermined position (for example, at the trailing 5 end of each code block) in each code block. In this case, redundant code bit sequences 19a and 19b which are the output of the encoder shown in Fig. 2 in the second embodiment are once held in a buffer and are collectively added in a predetermined code block 10 position. These characteristics of the invention on the recording information data sector are given as the characteristics of a recording code sequence format on the recording medium and in addition, the embodiment in the corresponding circuit can be verified for formats 15 of the write current sequence 105, the reproduced signal sequence 305 and the reproduced code sequence which are input/output to/from the recorded/reproduced signal processing circuit 1.

Fourth Embodiment

20 Fig. 4 shows an example of the configuration of an error correction decoder (an error-correction encoding circuit in decoding) 302 in the invention. In the decoder 302 equivalent to the fourth embodiment and shown in Fig. 4 corresponding to the second embodiment 25 shown in Fig. 2, a decoded signal sequence 303 which is output from the reproduced signal processing circuit 304 is input and data demodulation to a reproduced code information 301 is realized. In the decoder 302, a

maximum-likelihood detector 31 receives produced signal information (generally a sequence of a digital signal value) from the reproduced signal processing circuit 304 and determines a code bit information sequence corresponding to the reproduced signal information. Generally, in a recording/reproduction system using PRML, a digital signal sequence after partial response equalization by a digital filter is converted to hard-decision reproduced code bit information $\{a_k\}$ by the maximum-likelihood detector.

However, in the invention, as error correction based upon Turbo decoding is executed in a succeeding iterative detector 33, maximum posterior probability determination (maximum a posterior (MAP) decoding) matched with code detection for the partial response redundant system is executed in place of the maximum-likelihood detector and each code bit information is output as soft-output code information $\{b_k\}$ which is multivalued information shown by the reliability (probability) of the code bit. The algorithm of the MAP decoding and a concrete configuration method are widely disclosed in the nonpatent reference document 2 and a document ("Implementation and performance of a serial MAP decoder for use in an iterative turbo decoder", in Proc. IEEE International Symposium on Information Theory, September 1995, pp. 471) for example and further simplified various methods may exist, however, in the invention, the configuration of

the MAP decoding may be also formed by any method.

The soft-output code information sequence 32 output from the maximum-likelihood detector 31 by the MAP decoding is input to the iterative detector 33 (a 5 Turbo error correction decoder), error correction described in detail is performed and an error-correction decoded sequence 34 which is hard-decision bit information is output. A recorded code demodulator 35 is a circuit that executes coding demodulation of 10 reverse conversion corresponding to the recorded code modulator 12 shown in Fig. 2 and outputs a recorded demodulated code sequence 36. Further, an error-correction demodulator (demodulating circuit) 37 is a circuit that corrects a code error in the recorded 15 demodulated code sequence 36 using first error-correction coding (the redundant code 23) by the Reed-Solomon code and executes hard-decision error-correction decoding. Hereby, a reproduced code sequence 301 is regenerated.

20 In this embodiment, the error correction based upon Turbo decoding in the iterative detector (detection circuit) 33 is a first features. The soft-output code sequence 32 input to the iterative detector 33 is distributed into soft-output information 25 corresponding to an original information sequence code and soft-output information corresponding to each parity code bit (the redundant code bit 22b shown in Figs. 3 and 14) respectively added in the redundant

encoders (encoding circuit) 16a and 16b via a multiplexer 306. That is, the multiplexer 306 is a circuit that executes reverse operation to the code switch 20, divides a series of soft-output code sequence 32, memorizes and holds soft-output information equivalent to the original recording information of a user in a soft-output buffer 307 and respectively memorizes and holds soft-output information equivalent to each parity code bit 5 respectively added in the redundant encoders 16a and 16b in soft-output buffer circuits 307a and 307b. The soft-output buffer circuits 307a, 307b and 307c correspond to the code buffer circuits 15a, 15b and 15c, however, as processing delay time caused by succeeding 10 iterative decoding is required to be absorbed, memory size large enough than the code buffer circuit and the code block 22b is often required.

15

Further, at the succeeding stage, error-correction processing in units of the code block 22b is 20 executed using parity decoders (decoding circuits) 309a and 309b based upon the information held in the soft-output buffer circuits 307a, 307b and 307c.

In this embodiment, the parity decoder 309a corrects a code error using the redundant code bit 25 sequence 19a from the redundant encoder 16a shown in the encoder in Fig. 2 in the second embodiment. That is, the parity decoder 309a receives soft-output information 308 (user code information) equivalent to

the corresponding code block 22a in the soft-output
buffer circuit 307 and soft-output information (a
parity bit code soft-output information sequence 308a)
corresponding to the redundant code bit 22b (the parity
5 code information 19a by the redundant encoder 16a) of
the corresponding code block 22a held in the soft-
output buffer circuit 307a, and updates the input soft-
output information 308 (the user code information) to
more reliable information under a code constraint
10 condition of the corresponding parity. The similar
algorithm of MAP decoding to the maximum-likelihood
detector 31 can be used for the updating of reliability.
The soft-output information 308 of the corresponding
block 22a is updated and output (as an updated soft-
15 output block information sequence 310) by applying the
similar algorithm of MAP decoding, being matched with
the constraint condition of parity coding by the
redundant encoder 16a. A method of realizing MAP
decoding at high speed in the parity decoders 309a and
20 309b will be described in detail in a succeeding
embodiment.

Further, after the same interleaving (code
permutation) as the code block permutation (the code
permutation from the code buffer 15a to 15b) in the
25 random interleaver 15 in the encoder 102 is applied to
the updated soft-output information sequence 310 by a
random interleaver 313a, the soft-output information
sequence is supplied to the parity decoder 309b (as a

permuted soft-output block information sequence 311). That is, after reverse conversion (code permutation) to the predetermined code permutation is applied to the soft-output information sequence together with the 5 corresponding soft-output information generated based upon a reproduced signal sequence, decoding is repeated again using this and the permuted soft-output block information sequence 311 is supplied to the parity decoder 309b.

10 At this time, the parity decoder 309b corrects a code error using a constraint of the redundant code bit sequence 19b from the redundant encoder 16b. That is, the parity decoder 309a receives the supplied soft-output block information sequence 311 (the user code 15 information) and the parity code information 19b (a parity code soft-output information sequence 308b) of the corresponding code block 22a held in the soft-output buffer circuit 307b, and updates and outputs the input soft-output information 311 to more reliable 20 information under a code constraint condition of the corresponding parity as in the parity decoder 309a.

Further, reverse code permutation to the random interleaver 313a is applied to the soft-output information (an updated soft-output block information sequence 25 312) output at this time by a random interleaver 313b, a soft-output information sequence (a permuted soft-output block information sequence 314) corresponding to the code sequence of the original code

block 22a can be acquired and is fed back to the input of the parity decoder 309a again. As described above, the iterative decoder 33 is configured.

In iterative decoding, each information value of
5 the updated and feedback soft-output information sequence 314 is added to the corresponding information value of the soft-output information sequence 308 of the corresponding code block already held in the soft-output buffer circuit 307 (in an adder 314a) or the
10 permuted soft-output information sequence 314 is input to the parity decoder 309a as a newly revised soft-output information sequence 308. In the similar method to that described above, updated soft-output information is passed to the parity decoder 309b and
15 the updating of the information is repeated. In a process of the iterative decoding, to subtract duplication between information added in inputting and original information, a value of soft-output information added in inputting is required to be
20 subtracted from respective soft-output information values of the corresponding output in the output of each parity decoder 309a, 309b (in subtracters 314b and 314c).

As described above, a value of each soft-output information is gradually improved to high reliability by repeating permutation, updating the soft-output information sequence 308 of the corresponding code block between the parity decoders 309a and 309b. After

the repetition of parity decoding at a predetermined frequency, each value of the output soft-output information sequence 314 is compared with a predetermined value (in most cases, a value zero) by a 5 level detector 315 and is converted to a binary code value based upon the result. The result is output as the code information sequence of the corresponding block, is supplied to a recording code demodulator 35 as an error-correction decoded sequence 34 and reverse 10 code demodulation to the recording code modulator 12 is applied via the recording code demodulator. A recording demodulated code sequence 36 is output as reproduced code information 301 after error 15 detection/correction by first error-correction coding is further applied to the recording demodulated code sequence in an error-correction demodulator 37.

In the embodiment described above, corresponding to the coding shown in Fig. 2 in the second embodiment, in the detection/correction of a code error by second 20 error-correction coding, the detection and the correction of a code error using the soft-output information of each code bit generated based upon a signal sequence reproduced from the recording medium are performed, decoding corresponding to each parity 25 error-correction coding applied to each code sequence block is repeated again using the soft-output information generated based upon the reproduced signal sequence and the soft-output decoding information of

each code bit acquired based upon the result of another decoding. And after the above-mentioned process is repeated by a predetermined frequency, the result is output as the result of the reproduction of the 5 information code sequence. The error-correction processing means provided with the above-mentioned characteristics is provided in the invention.

Besides, for an error-correction decoding circuit, a soft-output decoder that receives a reproduced signal 10 sequence supplied from the recording medium and outputs the soft-output information of each code bit so as to detect and correct a code error by the second error-correction coding is provided. Each of plural error-correction decoding circuits that detect and correct a 15 code error using each the error-correction coding applied to each code sequence block receives the soft-output information of each code bit output from the soft-output decoder, receives soft-output information output from another error-correction decoding circuit, 20 repeats the detection and the correction of a code error of each code sequence block plural times and outputs the result as the reproduction of an information code sequence after the above-mentioned detection and correction of a code error are repeated 25 by a predetermined frequency (iteration number). The error-correction decoding circuit (the error-correction encoding circuit in reproduction) provided with the above-mentioned characteristics is provided.

Fifth Embodiment

Fig. 5 shows an example of the configuration of a random interleaver (circuit) having a feature of the encoder (the error-correction encoding circuit in recording) provided by the invention. As described above, the invention is characterized in that based upon the principle of Turbo coding, the generation and the addition of a parity redundant code are performed in units of code block 22a acquired by dividing the information code 22 in a recording information data sector in plurality. Therefore, in each code buffer circuit 15a or 15b for supplying a code to each redundant encoder 16a, 16b for generating parity, code registers 115a and 115b having a register length 115 equivalent to the length of a user recording information code in each code block 22a are provided. Further, to generate a parity redundant code by Turbo coding, predetermined code permutation way in which the order of held code information is permuted is applied between the code registers based upon pseudorandom regularity, afterward, the permuted code information in units of code block is serially input to the redundant encoder 16a or 16b and a 1- or more-bit redundant code is acquired.

Each code value of the recording modulated code sequence 13 input to the code buffer circuit (the recording buffer circuit) 15a or 15b provided with a function of an interleaver is sequentially input to the

code register 115a and is held, being shifted. Further, every time a code for one code block 22a is held in the code register 115a, the order of the contents of the held code value are permuted according to a 5 predetermined code permutation rule and the contents are copied in the code register 115b. The contents of the code register 115b are serially read out as the interleave output of the code buffer circuit 15a or 15b. Code permutation processing from the code register 115a 10 to 115b is executed with the length of a user recording information code in the code block 22a as a cycle and when a code value held at the input terminal of the code register 115a is sequentially shifted and is removed from the trailing end at the executed timing of 15 the code permutation processing, the next code permutation processing is executed. Further, the contents of the code delay element 17a, 17b in the corresponding redundant encoder 16a, 16b are reset to a predetermined initial value at the executed timing of 20 the code permutation processing. Hereby, the generation of a parity code is independently executed between each code block 22a.

It is desirable that the permutation of a code in 25 interleave in the code buffer circuit 15a or 15b complies with an ideal random permutation rule in case there is no regularity in the occurrence (event) of a code error, however, for example, in case event the probability of code errors in continuous bit positions

is remarkably high in a partial response transmission system, a code permutation rule is set so that the continuous bit positions are separated at as a distant interval as possible. For example, in a
5 recording/reproduction system in which a code error of N bits in length is frequently caused, a permutation rule is set so that at least two of continuous N-bit positions in the code register 115a are arranged in the code register 115b apart by a predetermined code
10 bit distance L or longer. At this time, if a parity redundant code is coded so that a redundant code bit (a parity coded bit) 22b is generated at an interval of L-1 bits for the code block 22a, an error code can be efficiently corrected by the iterative decoding.

15 Sixth Embodiment

An embodiment of parity coding according to the invention will be described below. When in the above-mentioned parity coding, a recording information code sequence $(x_0, x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, x_9)$ (x_i : binary code bit of 0 or 1) having 10-bit length is set in a code block 22a in the code register 115a of the code buffer circuit 15a, the result acquired by permuting the order of the code by interleave shall be
20 $(a_0, a_1, a_2, a_3, a_4, a_5, a_6, a_7, a_8, a_9)$. In case a redundant code block 22b is added every 5 bits when the code delay element 17a generates and outputs a redundant code sequence
25 $(pa_0, pa_1, pa_2, pa_3, pa_4, pa_5, pa_6, pa_7, pa_8, pa_9)$ based upon the input of the code using an odd-even single parity

(initial value: zero) as the redundant encoder 16a, a parity code is inserted every 5 bits in the code sequence and a code sequence for the corresponding code block 22a finally output from the encoder 102 is

5 $(x_0, x_1, x_2, x_3, x_4, \underline{pa}_4, x_5, x_6, x_7, x_8, x_9, \underline{pa}_9)$ (The underlined codes are equivalent to the redundant code bit 22b shown in Fig. 3).

Or a parity redundant code is arranged in the code block 22a or in a predetermined position in a recording information sector and for example, is collectively arranged at the trailing end of the block as $(x_0, x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, x_9, \underline{pa}_4, \underline{pa}_9)$ (The underlined codes are equivalent to a redundant code bit 22b shown in Fig. 14.). At this time, the parity redundant codes

15 \underline{pa}_4 and \underline{pa}_9 show the odd-even state of the codes (odd number or even number of emergent frequency of code 1) from the head of the permuted code sequence

10 $(a_0, a_1, a_2, a_3, a_4, a_5, a_6, a_7, a_8, a_9)$ to the code a_4 and the code a_9 , the parity decoder 309a that executes error 20 correction corresponding to the redundant parity on the reproduction side updates soft-output information by using a constraint condition of the odd-even state by the parity redundant codes for the soft output of the corresponding code block $(x_0, x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, x_9)$.

25 In addition to the case the single redundant encoder 16a is used as described above, the case that plural redundant encoders (parity coding) are used in parallel for coding is already shown in Fig. 2 in the

second embodiment. In this case, the second code
buffer circuit 15b that supplies an input code to the
second redundant encoder 16b executes interleave code
permutation different from the first code buffer
5 circuit 15a (Or in the first code buffer circuit 15a,
no code permutation is executed, the parity coding is
executed with the input code sequence as it is and in
the second code buffer circuit 15b, specific interleave
permutation is executed).

10 In this case, if plural parity coding is executed
under the similar coding condition, a code sequence
output from the encoder 102 is

$(x_0, x_1, x_2, x_3, x_4, \underline{pa}_4, \underline{pb}_4, x_5, x_6, x_7, x_8, x_9, \underline{pa}_9, \underline{pb}_9)$ (the
underlined code is equivalent to the redundant code bit
15 22b shown in Fig. 3) or

$(x_0, x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, x_9, \underline{pa}_4, \underline{pa}_9, \underline{pb}_4, \underline{pb}_9)$ (the
underlined code is equivalent to the redundant code bit
22b shown in Fig. 14) when the redundant encoder 16b
generates a redundant code sequence

20 $(pb_0, pb_1, pb_2, pb_3, pb_4, pb_5, pb_6, pb_7, pb_8, pb_9)$ for a code
permuted in the code buffer circuit 15b
25 $(b_0, b_1, b_2, b_3, b_4, b_5, b_6, b_7, b_8, b_9)$. In this case, the
respective soft-output information of the parity
redundant codes $(\underline{pa}_4$ and $\underline{pa}_9)$ and $(\underline{pb}_4$ and $\underline{pb}_9)$ is
independently used in the corresponding plural parity
decoders 309a and 309b, and the soft-output information
of the corresponding code block
 $(x_0, x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, x_9)$ is updated.

In this example, the number of parity redundant codes generated for the code block 22a by plural parity coding is the same, however, taking account of the redundancy of the whole code sequence, the number of 5 parity redundant code bits can be set to a different number every parity coding (redundant encoder). In the invention, three or more redundant encoders can be also provided in parallel and in each code buffer circuit 15a corresponding to these, desired performance can be 10 acquired by executing interleave conversion processing in order according to different code permutation rules based upon interleave configuration shown in Fig. 5 (Parity redundant coding is allocated to each code 15 information by the number of redundant encoders). In this case, as described in the embodiment shown in Fig. 4, the parity decoder 309a on the side of the decoder 302 are cascaded by the number of redundant encoders 16a, the result of soft output is sequentially received 20 and sent out to the following decoder, and iterative decoding is executed.

In the parity coding in each redundant encoder, a coding method of resetting the contents of the code delay element 17a to an initial value every time a parity redundant code is output from the redundant 25 encoder 16a can be also adopted. As described above, a code sequence of a code block after interleave input to each redundant encoder is $(a_0, a_1, a_2, a_3, a_4, a_5, a_6, a_7, a_8, a_9)$ and when pa_4 and pa_9 in a redundant code sequence

($pa_0, pa_1, pa_2, pa_3, pa_4, pa_5, pa_6, pa_7, pa_8, pa_9$) generated in response to the input of the code is added as redundant parity, the contents of the code delay element 17a are reset to an initial value zero at timing at which the 5 two redundant codes (pa_4, pa_9) are referred. At this time, coding is independently executed in a code sequence before and after resetting and the following code constraint condition comes into existence.

$$a_0 (+) a_1 (+) a_2 (+) a_3 (+) a_4 (+) \underline{pa_4} = 0 \\ 10 \quad a_5 (+) a_6 (+) a_7 (+) a_8 (+) a_9 (+) \underline{pa_9} = 0 \quad (1)$$

(Here, (+) denotes exclusive-or operation)

As described above, in this embodiment using single parity, in each parity coding, each information code bit a_1 belongs to one of code blocks constrained by respective generated parity redundant codes. When 15 pb_4 and pb_9 out of generated redundant parity are added to another interleave permuted code sequence ($b_0, b_1, b_2, b_3, b_4, b_5, b_6, b_7, b_8, b_9$), a code constraint condition comes into existence as in (1) as follows.

$$20 \quad b_0 (+) b_1 (+) b_2 (+) b_3 (+) b_4 (+) \underline{pb_4} = 0 \\ b_5 (+) b_6 (+) b_7 (+) b_8 (+) b_9 (+) \underline{pb_9} = 0 \quad (2)$$

Each information code is in different combination under the two code constraint conditions by different two-way (generally, plural) interleaving for a code 25 sequence and the update of the soft-output reliability of each code under one constraint condition contributes to the improvement of soft-output reliability by the other constraint condition.

As shown in above (1) and (2), the improvement of code soft-output information under the independently blocked code constraint condition can be realized by extremely simple algorithm. As described above, when a 5 code block $\{x_0, x_1, x_2, x_3, x_4, x_5\}$ is constrained under a condition $x_0(+)\bar{x}_1(+)\bar{x}_2(+)\bar{x}_3(+)\bar{x}_4(+)\bar{x}_5 = 0$, the soft-output maximum-likelihood information $\{r_0, r_1, r_2, r_3, r_4, r_5\}$ of each code in the code block is updated based upon the soft-output maximum-likelihood information 10 $\{\underline{r}_0, \underline{r}_1, \underline{r}_2, \underline{r}_3, \underline{r}_4, \underline{r}_5\}$ of each code before update by the following operation.

$$r_k = 2 * \operatorname{atanh}[(\prod_{i=0:5/k} \tanh(\underline{r}_i/2))] \quad (3)$$

($\prod_{i=0:5/k}$ shows the product of all elements of index i = 0 to 5 except k.)

15 Then, the soft-output maximum-likelihood is expressed by logarithmic probability maximum-likelihood ratio $r_k = \log [P(\text{probability that code value at time } k \text{ is 1})/P(\text{probability that code value at time } k \text{ is 0})]$, probability that if r_k is a positive value, its code 20 value is 1 and if r_k is a negative value, its code value is 0 is high and its absolute value denotes reliability the code value. The expression (3) shows that the decoding (updating) of each soft-output code information in each block under a code constraint can 25 be independently executed in parallel for extremely high speed operation at a single bit time interval.

As described above, as the independent and parallel update of soft-output information can be

applied to each code block to which a parity redundant code is added in case independent single parity coding in this embodiment is executed and operation for updating in an individual block can be executed at 5 extremely simple and short operation delay as shown in the expression (3), decoding delay time (latency) can be extremely short even if iterative decoding is executed between plural parity decoders 309a and 309b. In this embodiment of the invention, the extremely 10 effective method for making the enhancement of error-correction ability by Turbo decoding principle and the reduction of decoding delay time consist and the circuit for embodying the method are realized by independently applying one or more single parity coding 15 to a recording information block via interleave code permutation and executing iterative decoding between each parity code.

Seventh Embodiment

Fig. 6 shows the advantage of soft-output 20 decoding by single parity coding according to the invention. Fig. 6 is a trellis diagram used for MAP soft-output decoding in a parity decoder (decoding circuit) and arrows show a time course in the 2-state trellis diagram showing the odd-even state of a code 25 sequence. Fig. 6 is equivalent to a case that when a single parity redundant code sequence $(p_{a_0}, p_{a_1}, p_{a_2}, p_{a_3}, p_{a_4}, p_{a_5}, p_{a_6}, p_{a_7})$ is generated and output for an information code sequence $(a_0, a_1, a_2, a_3, a_4, a_5, a_6, a_7)$,

redundant codes pa_3 and pa_7 are added every 4 bits. The above-mentioned 8-bit information code sequence started at time k can have arbitrary state transition between two states (a constrained state (an even state) 5 400a and an odd state 400b) in the trellis diagram. As the initial state of the redundant encoder 16a is reset to either state (in this case, a state that the emergent frequency of a code 1 which zeroises a state of the code delay element 17a is even), a trellis initial 10 state before the time k is fixed to the constrained state (the even state) 400a.

Besides, as a recording information code sequence is forcedly constrained at an time interval of five bits by the insertion of added redundant codes pa_3 and pa_7 , a state of a trellis is forcedly transferred to 15 the constrained state (the even state) 400a after time bit $k+4$ and $k+9$ again. As a result, the trellis diagram is divided into two blocks (a parity coding block 400c) and this shows that the result of soft- 20 output decoding in one block has no effect upon output and update by soft-output decoding in the other block. Hereby, soft-output decoding (the update of soft-output 25 information) can be independently executed in every code block to which parity coding is applied and this means that parallel decoding every parity coding block is enabled. This is an effective advantage to reduce decoding delay time and to reproduce recorded information at high speed in the information

recording/reproducing apparatus.

In the above-mentioned seventh embodiment, the redundant encoder 16a mainly configured by the single code delay element 17a is used for the addition of parity redundancy used in the encoder 102, however, coding applied in this embodiment is not restricted to single parity coding. Further, in accordance with the characteristic of a code error, more general convolutional coding can be used.

10 Eighth Embodiment

Fig. 7 shows one example of the configuration of a convolutional encoder equivalent to an eighth embodiment of the invention and in the convolutional encoder (encoding circuit) 401, a shift register 402 that holds a 3-bit code is used for a code delay element. The contents of the shift register are sequentially shifted together with input to the input terminal 401a of the encoder and those contents show a state of the encoder. Further, the convolutional encoder 401 according to the invention is characterized in that the encoder has recursive configuration that exclusive-OR operation for the contents in a specific position of the shift register 402 feedback to input 401a to the encoder is carried out. Besides, the contents in a specific position of the shift register 402 are also referred for the output 401c of the encoder and the output is performed by sequentially operating the exclusive-OR operation for these contents

(exclusive-OR arithmetic elements 403a, 403b, 403c).

The above-mentioned single parity coding is the simplest example of the convolutional coding in case the shift register 402 is configured by a signal delay 5 element, however, as in the data demodulating system based upon the partial response method in magnetic recording, in the case of a demodulation system in which a single- or an odd-bit code error events are frequently caused, relatively simple and efficient 10 error-correction coding is provided. Further, for the more complex pattern of a code error event caused in a reproduced data sequence, the error event can be securely detected and corrected by applying the convolutional encoder 401 having more complex 15 configuration as the redundant encoders 16a and 16b of the encoder 102.

For example, when the whole contents of the shift register 401 of the convolutional encoder are reset to zero and a supposed error pattern (a pattern sequence 20 in which an error bit position is 1 and a normal code bit position is 0) is provided as input 401a to the encoder, the code error event with the error pattern can be detected by the convolutional coding if the whole contents of the shift register are not reset to 25 zero finally. The application of the encoder having recursive configuration in the invention provides effect to induce error propagation in a reproduced data sequence and to facilitate the detection of a code

error event when interleaving the reproduced data sequence.

Ninth Embodiment

For a further embodiment of the invention, exists an embodiment of decoding that after the detection and correction of a code error using the soft-output information for each code bit generated based upon a reproduced signal sequence from the recording medium by second error-correction coding by single parity coding or by second error-correction coding by iterative decoding between plural parity codes as described above, the soft-output decoding information for each code bit is fed back to the maximum-likelihood detector 31 again and the soft-output coding information for each bit in the corresponding information data sector is regenerated based upon the reproduced signal sequence and the feedback soft-output decoding information. Fig. 10 shows another embodiment of the error-correction decoder.

In a decoder 302 equivalent to this embodiment, a part encircled by a dotted line (an iterative decoder) 33 has basically the similar configuration and operation to that of the decoder in the fourth embodiment shown in Fig. 4. In a normal mode, the output terminal of a switch 317 is connected to the side of 312 according to an instruction signal 317a and the output of a parity decoder 309b is fed back as input information to a prior parity decoder 309a. In this

state, in a system provided with plural parity decoders (parity coding) as shown in Fig. 10, as in the embodiment shown in Fig. 4, the input/output of soft-output code information between the parity decoders is 5 repeated and soft-output reliability for each code bit is improved. After a predetermined iterative frequency, the output result is supplied to a level detector 315 via 314, is converted to an error-correction decoded sequence 34 to be the result of decoding.

10 The ninth embodiment is characterized in that after parity decoding is repeated up to a predetermined frequency (iteration number), the soft-output code information updated by the parity decoding for each code bit in the corresponding recording information 15 data sector is feedback to a maximum-likelihood detector 31 again and the soft-output information for each code bit is reconfigured using the soft-output information for each code bit (soft-output code information 320b) together with the information of a decoded signal 20 sequence 303 to further improve the reliability of decoding. Such a maximum-likelihood detector 31 is characterized in that feedback soft-output code information 320b the reliability of which is updated by the parity decoding is input again as the prior 25 probability of each code bit information and is used in the maximum-likelihood detector 31.

Hereby, in the maximum-likelihood detector 31 that is matched with a partial response transmission

system and evaluates posterior probability of each data code bit, the reliability deterioration of soft-output code information due to error propagation can be avoided. That is, if a code error bit corresponding to 5 at least a part of error propagation is detected and the reliability of the code error bit can be improved by parity decoding, whole the continuous code error event due to error propagation caused in maximum-likelihood decoding which uses redundancy of 10 intersymbol interference in the partial response transmission system and the deterioration at a burst of code bit reliability can be removed. Further, hereby, if the burst code error is improved, error-correction ability can be more effectively used for correcting a 15 residual random bit code error in parity decoding executed again at the succeeding stage of the maximum-likelihood detector 31. As described above, the combination of the correction (first iterative decoding) for a random short error event by parity decoding and iterative decoding (second iterative decoding) in which maximum-likelihood decoding matched with the partial response transmission system is repeated can very efficiently correct a code error 20 event in a realistic recording/reproduction system.

25 Tenth Embodiment

An example showing the adjustment of ability for correcting a random code error according to the invention will be described as a tenth embodiment below.

Feedback decoding (second iterative decoding) to the maximum-likelihood detector 31 using the result of iterative parity decoding can improve the reliability of the whole decoding system further at the maximum by 5 suitably setting a frequency of the inner iterative decoding (first iterative decoding) between plural parity codes shown in the inside (33) of the dotted line shown in Fig. 10 and adjusting the capability for correcting a random code error event. As described 10 above, for the inner iterative decoding (the first iterative decoding) between plural parity codes inside the dotted line, decoding in units of code block and high-speed decoding processing by parallelization are enabled and as the decoding processing is enabled at 15 the delay of time for a few bits, a frequency of the two iterative decoding can be more flexibly set against the constraint of decoding delay time in a realistic high-speed recording/reproduction system.

The embodied configuration of the first iterative decoding is shown inside the dotted line shown in Fig. 20 10 (33) or is shown in Fig. 4 related to the fourth embodiment. Besides, the embodied configuration of the second iterative decoding is shown in Fig. 10 and the output of feedback soft-output code information (user 25 recorded information) 318 from the switch 317 is feedback to the maximum-likelihood detector 31. To feedback the feedback soft-output code information to the maximum-likelihood detector 31, parity code

feedback soft-output information sequences 318a, 318b are required to be inserted in original code positions of the feedback soft-output code information (user recorded information) 318 of the corresponding code 5 block and one feedback soft-output code information sequence for each code block is required to be reconfigured. It is a demultiplexer 319 that executes this and the soft-output code information 318a, 318b (each output of the parity decoders 309a and 309b) of 10 the corresponding parity code are inserted in predetermined positions of the feedback soft-output code information (user recorded information) of each code block, that is, code sequence conversion opposite to the multiplexer 306 is executed. Hereby, the 15 configured feedback soft-output code information (user recorded information) of each code block is sent to the maximum-likelihood detector 31 as the prior probability information for each code bit.

Further, in the tenth embodiment, to efficiently 20 apply parity correction to code error propagation which may occur in the maximum-likelihood detector 31 at the succeeding stage, permutation may be applied to a soft-output code information sequence 32a output from the maximum-likelihood detector 31 by an interleaver 316a. 25 The interleaver 316a converts code bit arrangement so that soft-output code information output in a continuous code bit position on 32a is related to as different parity checks as possible, and facilitates

the detection of a part of a burst code error event from the maximum-likelihood detector 31 by the parity decoding using soft-output code information 32b output from the interleaver.

5 In the second iterative decoding, the possibility of burst error correction can be enhanced by the effect. The unit (block size) of permutation by the interleaver 316a is a single or plural blocks in units of code block 22a and further, may be also an 10 information data sector (The unit is set depending upon the extent of error code propagation allowed when the second iterative decoding is executed, and the determination of the unit of permutation and the effect 15 of improving a burst error correction are in the relation of trade-off).

 In this case, in the second iterative decoding, a deinterleaver 316b for applying reverse processing for restoring permutation by the interleaver 316a to feedback soft-output code information 319b output from 20 the demultiplexer is provided and hereby, feedback soft-output code information 320b permuted in original code order is supplied to the maximum-likelihood detector 31. In case soft output from the maximum-likelihood detector 31 is permuted by interleave as in 25 this embodiment, recording code bit information is permuted in recording beforehand and is recorded on the recording medium so that parity decoding at the succeeding stage is suitably executed and the order of

permuted code bits complies with a format of parity coding shown in Fig. 3.

Eleventh Embodiment

Fig. 8 shows an example of a recording encoder 5 showing the permutation of a recording code sequence according to the invention at this time and an interleaver 21 for executing code permutation processing reverse to the interleaver 316a is provided before the output terminal of a recording code sequence 103 and the recording code bits are recorded in the order of permuted codes. In case the interleaver 316a is provided to the encoder 302 in the embodiment shown in Fig. 10, with such prior permuting for the recording code sequence, error correction in parity decoding in 15 the inside of the dotted line at the succeeding stage can be executed by the above-mentioned method .

Twelfth Embodiment

Fig. 9 shows another example of processing for 20 permuting a recording code sequence according to the invention and shows an example of the configuration of a recording encoder that applies code permutation to a recording modulated code sequence 13 and a recording code sequence before being input to a concatenated encoder 14 by a predetermined interleaver 22 to prevent 25 violating code constraint by the interleaver 21 and produces the similar effect to that in the eleventh embodiment shown in Fig. 8. By this equivalent code permutation, the interleave 316a can be also omitted on

the side of the decoder 302 and a problem of error propagation in iterative decoding can be avoided. For second iterative decoding, the possibility of the deterioration of reliability due to the above-mentioned
5 error propagation can be reduced by using second iterative decoding only in case error correction 37 by first error-correction coding cannot correct all code errors.

Hereby, in the interleaver 22 shown in Figs. 9
10 and 8, to enhance the effect of the second iterative decoding, it is desirable that the unit (interleaver size) of code permutation is set to as a large size as possible. For the unit (interleaver size) plural code block sizes or length equivalent to information data
15 sector length can be selected. Under such a condition, the configuration of the encoder equivalent to the embodiment shown in Fig. 9 is characterized in that after code permutation is applied to a code sequence to which first code error-correction coding is applied,
20 the second error-correction coding is executed.

In Figs. 8 to 10, the embodiments are described using the concrete examples in which plural parity coding are used in every unit of code block shown in Fig. 3, however, the invention can be also easily
25 applied to a case that single error-correction coding (parity coding) is used in each code block.

Thirteenth Embodiment

Fig. 11 shows an example of a recording encoder

in case single parity coding is applied to each code block and the recording encoder is similarly operated corresponding to that equivalent to the eleventh embodiment shown in Fig. 8 (It similarly corresponds to 5 that equivalent to the twelfth embodiment shown in Fig. 9). In a thirteenth embodiment, a single code buffer circuit 15a and a single redundant encoder 16a are provided and a redundant code by single parity coding is inserted into each code block shown in Figs. 3 and 10 14. Fig. 12 shows the configuration of a decoder 302 corresponding to the encoder 102 and a single parity decoder 309a is provided in this decoder 302. Iterative decoding at this time is mainly executed by the above-mentioned second iterative decoding. 15 Therefore, a soft-output block information sequence 310 updated in the parity decoder 309a is feedback to a maximum-likelihood detector 31 via a switch 317 and a demultiplexer 319 in iterative decoding and is iteratively processed as described above. After the 20 iteration by a predetermined frequency (iteration time), the soft-output block information sequence 310 is supplied to a level detector 35 according to an instruction signal 317a and is output as the result of decoding. In the case of the iteration in such single 25 parity decoding, the similar effect of correcting both a random code error event and a burst error event to that in the above-mentioned embodiments can be expected by limiting the unit size of code permutation in a code

buffer circuit 15a and an interleaver 316a to the unit of a code block described in relation to Figs. 3 and 14.

As described in this thirteenth embodiment and the tenth embodiment shown in Fig. 10, one of the features of an information recording/reproducing coding method and an information recording/reproducing encoding circuit according to the invention is in that soft-output decoding information for each code bit is regenerated using soft-output decoding information for each code bit acquired after decoding by second error-correction coding in the detection and correction for a code error in each information data sector together with a reproduced signal sequence from the recording medium, and error correction by the second error-correction coding is repeated using this regenerated soft-output decoding information. A coding method corresponding to this decoding is characterized in that after predetermined code permutation processing (in most cases, in a unit (permutation block size) equivalent to length of a recording information data sector) is applied to a code sequence to which first error-correction coding is applied, second error-correction coding is applied.

Besides, the information recording encoding/decoding circuit according to the invention is characterized in that a code permutation circuit that holds and permutes an output code acquired by adding a redundant code to an output code sequence from an

encoding circuit which applies first error-correction coding, is provided, processing by the second error-correction encoding circuit is applied to a code sequence output from the code permutation circuit, a reproduced signal sequence supplied from the recording medium is input to a circuit for detecting and correcting a code error in an information code sequence, a maximum-likelihood decoder to which the information of soft-output decoding for each code bit supplied from the error correcting circuit by second error-correction coding is input is provided, soft-output decoding information by second error correction is input again, the soft-output decoding of each code bit is executed by a predetermined frequency (iteration number) and code correction processing by the second error-correction coding is repeated.

As described above, as the iterative decoding in the invention is executed in iteration units of information data sector, decoding delay time (latency) often comes into practical issue when this embodiment is applied to a realistic information recording apparatus. As in the invention, an error-correction demodulator 37 by hard decision for first error-correction coding such as a Reed-Solomon code together with the iterative decoding is provided, a data recovery method is enable, in which the second iterative decoding only in case a code error is detected in the first error-correction coding and all

code errors cannot be corrected (only in a retry operation mode in hard-disk drive). By using this method, the iteration number of code error detection and correction (first iterative decoding) by first 5 error-correction coding or the iteration number of code error detection and correction by second error-correction coding can be also reduced to a necessary and minimum number of iteration. This is an effective method for reducing power consumption and data access 10 time in the circuit or the recording/reproduction apparatus to which the invention is applied. Then the circuit for embodying the method is available.

Besides, in case an integrated circuit is mounted for such an information recording encoding circuit, an 15 iterative frequency or the maximum iterative frequency of detecting and correcting a code error by the first error-correction coding or by the second error-correction coding is set from the outside of the information recording encoding circuit. One of 20 features of the integrated circuit mounted in the invention is in that a memory circuit or a register for setting and holding the iterative frequency and an interface for setting the iterative frequency to the memory circuit is/are provided. This is required to 25 specify the maximum decoding delay time (latency) of the information reproducing circuit for a host recording/reproducing controller.

The information recording/reproducing circuit

provided by the invention can be mounted on a large-scale integrated circuit (LSI) in the above-mentioned embodiment. In addition, this small-sized LSI component can be easily applied to an information

5 recording/reproduction apparatus for which high speed and high density are required such as a magnetic hard disk drive unit.

Fourteenth Embodiment

Fig. 13 shows an example of the configuration of a magnetic recording/reproduction apparatus according to the invention. A magnetic disk recording medium 95 in which a recording layer 91 for magnetically recording information is formed on a substrate is turned by a spindle motor 93 and a magnetic head slider 90 provided with a magnetic sensor film is guided on a track of the magnetic disk recording medium 95 by an actuator 92. In the magnetic recording/reproduction apparatus, a magnetic recording head and a magnetic reproducing head respectively mounted on the head slider 90 as a magnetic sensor are positioned in a predetermined recording position on the magnetic disk recording medium by the above-mentioned mechanism and the magnetic recording head sequentially writes a signal, relatively being moved or the magnetic reproducing head reads a written signal. A recording signal is recorded on the magnetic disk recording medium 95 by the magnetic recording head via a recording/reproduced signal processing system 94 and in

the case of reproduction, the output of the magnetic reproducing head is acquired as a signal via the signal processing system 94. In Fig. 13, one head slider 90 and one magnetic disk recording medium are shown,

5 however, respective plural ones may be also provided.

The magnetic disk recording medium 95 may be also provided with the recording layer 91 on both sides. In case information is recorded on both sides, the head slider 90 is arranged on both sides of a disk.

10 For the recording/reproduced signal processing system of the magnetic recording/reproduction apparatus, the information recording/reproducing encoding circuit according to the invention is mounted. By mounting the information recording/reproducing encoding circuit
15 according to the invention, when signal amplitude loss (dropout) of predetermined code length is (intentionally) added to a reproduced signal sequence supplied from the magnetic disk recording medium or when an iterative frequency set from out of the
20 information recording /reproducing circuit is increased, the time interval since the reproduced signal sequence is input to the circuit until the decoding result of an information code sequence for the corresponding reproduced signal sequence is output from the circuit
25 increases by the increase of an iterative decoding frequency executed in the circuit. Similarly, when the code code error detection and correction by first error-correction coding do not function and signal

amplitude loss (dropout) of predetermined code length is (intentionally) added to a reproduced signal sequence supplied from the recording medium, a code error caused in the decoding result of an information 5 code sequence is longer than the length of the added signal amplitude loss and is caused in a limited length equal to or shorter than the code sequence block length in case the length of the signal amplitude loss exceeds a certain length equal to or shorter than code sequence 10 block length. Further, the configuration equivalent to the above-mentioned embodiment is also characterized in that the configuration in the above-mentioned embodiment that in the code error detection and correction by first error-correction coding, when a 15 flag showing that an error correction code is impossible is sent out, time interval since a reproduced signal sequence is input to the circuit until the decoding of an information code sequence is output to the circuit for the corresponding reproduced 20 signal sequence increases or the increase of time interval until the decoding result of an information code sequence for the corresponding reproduced signal sequence is output is equal to or shorter than time interval in which the code contents in the whole 25 corresponding information data sector are output.

The above-mentioned characteristics are suitable to apply iterative decoding according to the invention and secure the data reliability reproduced from of a

magnetic hard-disk drive unit when the contents of a predetermined recorded information data sector on a medium cannot be completely read out in one reproduction processing in the magnetic disk unit to 5 which the invention is applied, that is, in case rereading in a retry mode is executed. Hereby, the enhancement of both the reproduction reliability of recorded data and the access performance/throughput can be realized in a mass-storage high-density magnetic 10 recording/reproduction apparatus.

An information recording/reproduction apparatus and an information communication device on which the information recording/reproducing encoding circuit according to the invention is mounted can also realize 15 the similar characteristic to the above-mentioned magnetic recording/reproduction apparatus.

Fifth Embodiment

It is verified that another embodiment of the invention can realize more powerful and higher-speed 20 error-correction coding to which the principle of Turbo coding is applied by the following each information recording/reproducing method.

The information recording/reproducing coding method is based upon an information 25 recording/reproducing coding method for recording/reproducing an information code sequence onto/from an information recording medium to which error-correction coding for detecting and correcting a

code error caused in the information code sequence reproduced from the information recording medium is applied (on the information recording medium) and is characterized in that error correction in units of 5 predetermined code (code symbol units) is executed in the unit (an information data sector) of an information code sequence once recorded on the information recording medium, first error-correction coding in which error code symbols equal to or smaller than a 10 predetermined number of code symbols caused in the corresponding reproduced information data sector are corrected is executed, redundant codes or a redundant code sequence hereby acquired are/is added to the information data sector, the information data sector to 15 which the first error-correction coding is applied is divided into continuous plural code sequence blocks each of which has predetermined length of the code symbols, second error-correction coding is applied to each the code sequence block, redundant codes hereby 20 acquired are inserted to the corresponding code sequence block, the code sequence block to which the second error-correction coding is applied has a code sequence block length in units of code symbol in the first error-correction coding , the code sequence block 25 to which the second error-correction coding is applied has a code sequence block length equal to or shorter than the number of code symbols correctable by the first error-correction coding, and the information code

sequence to which the first and the second error-correction coding are applied is recorded on the information recording medium.

Besides, the information recording/reproducing coding method is characterized in that in the second error-correction coding, code permutation processing in a processing unit of code symbol length equal to the above-mentioned code sequence block is applied to a code sequence corresponding to the code sequence block, plural code sequence blocks from a code sequence are generated by the code permutation processing, predetermined error-correction coding is applied to each of the generated plural code sequence blocks and redundant code bits generated by respective error-correction coding are inserted into predetermined positions in the corresponding code sequence block.

The information recording/reproducing coding method is characterized in that in the code error detection and correction by the second error-correction coding, the code error detection and correction using the soft-output information of each code bit generated based upon a reproduced signal sequence from the recording medium is executed, decoding processing for the code error detection and correction is repeated again using the soft-output information generated based upon the reproduced signal sequence and the information of soft-output decoding for each code bit acquired as a result of another decoding for the code error detection

and correction corresponding to each error-correction coding applied to each code sequence block and after the above-mentioned processing is repeated by a predetermined frequency, the result is output as the 5 result of the reproduction of the information code sequence.

The information recording/reproducing coding method is characterized in that code permutation processing is executed in a processing unit of 10 information data sector length acquired by adding a redundant code to a code sequence to which the first error-correction coding is applied is executed.

The information recording/reproducing coding method is characterized in that in the second error- 15 correction coding and the detection and correction of a code error for the corresponding information data sector, the information of soft-output decoding for each code bit is regenerated using a reproduced signal sequence from the recording medium and the information 20 of soft-output decoding for each code bit acquired after the decoding processing by the predetermined frequency and the second error-correction coding is repeated using this regenerated information of soft-output decoding.

25 The information recording/reproducing coding method is characterized in that the code error detection and correction by the first error-correction coding or the code error detection and correction by

the second error-correction coding is repeated only in case a code error is detected by the first error-correction coding and all the code errors cannot be corrected.

5 The information recording/reproducing coding method is characterized in that the information recording medium is a magnetic disk recording medium.

According to the invention, the recording format for information data provided with more powerful and
10 higher-speed error-correction encoding means applying the principle of Turbo coding, the information recording/reproducing coding method and encoding circuit, the magnetic recording/reproduction apparatus using these, the information recording/reproduction
15 apparatus and the information communication device can be provided.